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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,211	07/08/2003	Toshihiro Kawakami	1504.1020	7319
21171	7590	01/19/2005	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005				NGUYEN, TANH Q
ART UNIT		PAPER NUMBER		
		2182		

DATE MAILED: 01/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/614,211	KAWAKAMI ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Tanh Q. Nguyen	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 08 July 2003.

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 1-5 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-5 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 08 July 2003 is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)  All   b)  Some \* c)  None of:

1.  Certified copies of the priority documents have been received.
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 07/08/03.

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-4 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by **Goodrum (USP 6,260,095)**.

3. As per claim 1, Goodrum teaches a data transfer controller [106, FIG. 1A] connecting a high-speed bus [110, FIG. 1A] having a relatively high data transfer rate [PCI bus: col. 5, lines 21-23] to a low-speed bus [112, FIG. 1A] having a relatively low data transfer rate [EISA bus: col. 5, lines 21-23], the controller comprising:

an address register [208, FIG. 2A; col. 6, lines 46-55; col. 7, line 66-col. 8, line 14] for storing an address allotted to a peripheral device [RSRV\_BASE\_ADDR and RSRV\_LIMIT\_ADDR being associated with the data to be retrieved from a peripheral device, hence the address of the data being allotted to a peripheral device] connected to the low-speed bus [112, FIG. 1A - As Goodrum contemplates read operations in the opposite direction (of memory read requests from downstream bus masters), Goodrum contemplates (downstream peripheral device) read requests from upstream bus masters, col. 7, lines 23-31, hence the address register storing an address allotted to a

peripheral device connected to the low-speed bus], the stored address being referred to as a preset address;

a buffer [206, FIG. 2A; col. 6, lines 46-49] for storing a data retrieved from the peripheral device based on the preset address [col. 7, line 6-col. 8, line 14; col. 9, lines 9-13; col. 9, lines 49-58], the retrieved data being referred to as prefetched data; and

a central controller [106, FIG. 1A] for causing the prefetched data stored in the buffer to be outputted into the high-speed bus when a peripheral device address transmitted through the high-speed bus is identical to the preset address [Goodrum teaches delayed (read) transactions being used with buffer reservations to improve performance (col. 11, lines 8-11); Goodrum teaches buffer reservation (i.e. storing an address in the address register and storing data in the buffer above); in the delayed transaction, the prefetched data stored in the buffer is outputted into the high-speed bus (col. 10, line 65-col. 11, line 3), when the bus master reissues the original (first phase: col. 10, lines 37-43) read request (downstream peripheral device read request) in the third phase (col. 10, line 65-col. 11, line 3), the reissued read request latching the transaction information required to complete the access (col. 10, lines 42-43, i.e. including a peripheral device address, which is identical to the address(preset address) in the address register) - hence the prefetched data stored in the buffer being caused to be outputted into the high-speed bus when a peripheral device address transmitted through the high-speed bus is identical to the preset address].

4. As per claims 3-4, Goodrum teaches the high-speed bus and the low-speed bus being arranged within a computer [100, FIG. 1A];

the high-speed bus [110, FIG. 1B] being arranged within a computer [100, FIG. 1B], the low-speed bus [112, FIG. 1B] being a cable arranged outside of the computer [FIG. 1B; col. 5, lines 28-36].

5. As per claim 5, Goodrum teaches a method for transferring data between a high-speed bus [110, FIG. 1A] having a relatively high data transfer rate [PCI bus: col. 5, lines 21-23] and a low-speed bus [112, FIG. 1A] having a relatively low data transfer rate [EISA bus: col. 5, lines 21-23], the method comprising the steps of:

storing an address allotted to a peripheral device connected to the low-speed bus, the stored address being referred to as a preset address (see rejection to claim 1 above);

storing a data retrieved from the peripheral device based on the preset address, the retrieved data being referred to as prefetched data (see rejection to claim 1 above); and

causing the stored prefetched data to be outputted into the high-speed bus when a peripheral device address transmitted through the high-speed bus is identical to the preset address (see rejection to claim 1 above).

#### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Goodrum** in view of **Seki et al. (USP 6,832,227)**.

Goodrum discloses the invention except for the address register holding an address (of data) having a relatively high access frequency.

**Seki** teaches high access frequency data being stored in a buffer memory for providing high-speed access to the data (col. 6, lines 58-62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the address register to hold an address (of data) having high access frequency in order allow high access frequency data to be prefetched in the buffer.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tanh Quang Nguyen whose telephone number is (571) 272-4154 and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin, can be reached on (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 for After Final, Official, and Customer Services, or (571) 273-4154 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Effective May 1, 2003 are new mailing address is:

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Art Unit: 2182

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.

*Christopher J. Kaul*  
01/14/2005

TQN  
January 12, 2005